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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
YAARY, MICHAEL D	
ART UNIT	**PAPER NUMBER**
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,796	LANGHAMMER, MARTIN	
	Examiner	Art Unit	
	Michael Yaary	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 11-19, 24-27, and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita et al. (hereafter Narita)(US Pat. 5,293,558) in view of Yu et al. (hereafter Yu)(US Pat. 6,523,055).

4. Yu was cited in the previous office action dated 07/23/2007.

5. **As to claims 1 and 14,** Narita discloses a multiplication unit, comprising a 2N-bit multiplier (multiplier 10 of figure 1) and having a first short word length multiplication mode (column 4, lines 29-30) and a second long word length multiplication mode (column 10, lines 43-44), wherein a short word length is N and a long word length is 2N

(column 4, lines 29-30 and column 10, lines 43-44), wherein N is an integer, and wherein :

In the first mode for multiplying two N-bit numbers, a first long word length multiplicand and a second long word length multiplicand are multiplied together using the 2n-bit multiplier to form a result (Column 4, lines 29-63 and figures 1-3 disclose n-bit by n-bit multiplication using a 2n-bit multiplier to output a 2n-bit result);

in the second mode for multiplying two 2N-bit numbers, wherein a third long word length is multiplicand is formed from a first pair of short word length words and a fourth long word length multiplicand is formed from a second pair of short word length words (Column 10, lines 43-65 and figure 12 disclose two 2n-bit words, comprised of X_L, X_H, Y_L, and Y_H), first words of the first and second pairs of short word length words are stored in respective registers connected to the 2N-bit multiplier (Figure 10, and column 9, lines 45-54), and subsequently the third and fourth long word length multiplicands are multiplied together using the 2N-bit multiplier (multiplication done at multiplier 10 of figure 10).

6. Narita does not disclose that in the first mode, a first long word length multiplicand is formed from a first short word length multiplicand, and a second long word length multiplicand is formed from a second short word length multiplicand.

However, in an analogous art, Yu discloses a first long word length multiplicand is formed from a first short word length multiplicand, and a second long word length multiplicand is formed from a second short word length multiplicand (Column 6, line 54-

column 7, line 7 disclose a multiplier circuit in which multiplicands generate intermediate products wherein sign extension and zeroing are performed to properly align inputs for multiplication. Thus, analogously, these extending techniques may be implemented in the teachings of Narita, to extend two N bit short words into long word lengths).

7. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the teachings of Narita, by extending and zeroing multiplicands in a multiplication circuit, as taught by Yu, for the benefit of effectively aligning two N-bit multiplicands in a first multiplication state.

8. **As to claim 26,** the claim is rejected for the same reasons as claim 1 and 14 above.

9. **As to claims 2 and 15,** the combination of Narita and Yu disclose in the first mode, the first long word length multiplicand is formed as a sign extended version of the first short word length multiplicand, and the second long word length multiplicand is formed as a sign extended version of the second short word length multiplicand (Yu, column, 6, lines 54-58 disclose sign extension of a multiplicand, but not necessarily performed on both multiplicands. However, it would have been obvious to one of ordinary skill in the art to apply sign extension to the multiplicands as necessary for correct aligning.).

10. **As to claims 3 and 16,** the combination of Narita and Yu disclose in the first mode, the first long word length multiplicand is formed from the first short word length multiplicand plus zeroes as the most significant bits, and the second long word length multiplicand is formed from the second short word length multiplicand plus zeroes as the most significant bits, such that the multiplication result includes an unsigned product of the first and second short word length multiplicands (Yu, column 6, lines 54-58 disclose sign-extension performed, but does not explicitly disclose the sign-extending includes adding zeroes to the most significant bits. However, it is well-known knowledge in the art, that sign-extension on binary values is done by adding zeroes the most significant bits to increase the number of bits of a binary number. Thus, it would have been obvious to one of ordinary skill in the art to apply zeroes as the most significant bits of the first and second short word lengths as necessary, to correct aligning.).

11. **As to claims 4 and 17,** the combination of Narita and Yu disclose in the first mode, the first long word length multiplicand is formed from the first short word length multiplicand plus zeroes as the least significant bits, and the second long word length multiplicand is formed from the second short word length multiplicand plus zeroes as the least significant bits, such that the upper bits of the multiplication result contain the product of the first and second short word length multiplicands (Yu, column 6, lines 58-61 disclose zeroing least significant bits of a multiplicand, but not necessarily performed on both multiplicands. However, it would have been obvious to one of ordinary skill in the art to apply zeroing to the multiplicands as necessary for correct alignment.).

12. **As to claims 5 and 18,** the combination of Narita and Yu disclose in the second mode, second words of the first and second pairs of short word length words are stored in respective registers, before the third and fourth long word length multiplicands are multiplied together (Narita, column 4, lines 32-34 disclose two registers for holding values used for multiplying, thus storing the necessary values used in the circuit prior to multiplying.).

13. **As to claims 6 and 19,** the combination of Narita and Yu disclose a register file, from which the first and second short word length multiplicands, and the first and second pairs of short word length words, can be retrieved (Narita, figure 1 discloses two source registers 12 and 13).

14. **As to claim 27,** the combination of Narita and Yu disclose in the second mode of operation, the fifth and sixth data words of the first length are stored in respective multiplication registers after retrieval from the register file (Narita, column 4, lines 32-34 disclose two registers for holding values used for multiplying, thus storing the necessary values used in the multiplication circuit.).

15. **As to claims 11, 12, 24, 25, 31, and 32,** the combination of Narita and Yu disclose the short word length is 16 bits or 18 bits, and the long word length is 32 0r 36 bits (Narita, column 4, lines 29-30; and column 10, lines 43-44 disclose a 2n multiplier

for n by n multiplication and for 2n by 2n multiplication. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize any range of n bits and 2n bits accordingly as can fit in the data memory.).

16. **As to claim 13,** the claim is rejected for the same reasons as claims 1 and 3 above.

17. Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita in view of Yu as applied to claims 6 and 19 above, and further in view of Henderson et al. (hereafter Henderson)(US Pat. 6,484,194).

18. Henderson was cited in the previous office action dated 07/23/2007.

19. **As to claims 7 and 20,** the combination of Narita and Yu do not disclose the register file is a dual ported register file, such that:

In the first mode, the first and second short word length multiplicands can be retrieved at the same time, and in the second mode, first words of the first and second pairs of short word length words can be retrieved at a first time, and second words of the first and second pairs of short word length words can be retrieved at a second time.

However, Henderson discloses a dual ported register file (column 13, lines 39-44), such that:

In the first mode, the first and second short word length multiplicands can be retrieved at the same time, and in the second mode, first words of the first and second pairs of short word length words can be retrieved at a first time, and second words of the first and second pairs of short word length words can be retrieved at a second time (Column 13, lines 39-61 and figure 5b disclose a multiplication circuit utilizing dual ported registers to access data in different cycles. Thus, when combined with the teachings of Narita and Yu, may be implemented to read different word sets and the same or different times.

20. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Narita and Yu, by implementing a dual ported register file, as taught by Henderson, for the benefit of maintaining fast execution time in the multiplier circuit.

21. Claims 8-10, 21-23, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita in view of Yu as applied to claims 1, 14, and 26 above, and further in view of Bosshart (US Pat. 4,754,421).

22. Bosshart was cited in the previous office action dated 07/23/2007.

23. **As to claims 8, 21 and 28,** the combination of Narita and Yu do not disclose first and second long word length accumulators, for receiving the multiplication results.

However, in an analogous art, Bosshart discloses first and second long word length accumulators, for receiving the multiplication results (Column 3, lines 2-8 and figure 1 disclose accumulators A and B receiving multiplication results, and when combined with the teachings of Narita and Yu, can be implemented as long word length accumulators accordingly.).

24. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Narita and Yu, by implementing first and second accumulators, as taught by Bosshart, for the benefit of immediately being able to store multiplication results.

25. **As to claims 9, 22, and 29,** the combination of Narita, Yu, and Bosshart disclose in the second mode, the result of multiplying together third and fourth long word length multiplicands can be divided between the first and second long word length accumulators (Bosshart, column 4, lines 25-54).

26. **As to claims 10, 23, and 30,** the combination of Narita, Yu, and Bosshart disclose in the second mode, a selected part of the result of multiplying together the third and fourth long word length multiplicands can be stored in a selected one of the first and second long word length accumulators (Bosshart, column 4, lines 25-54).

Response to Arguments

27. Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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